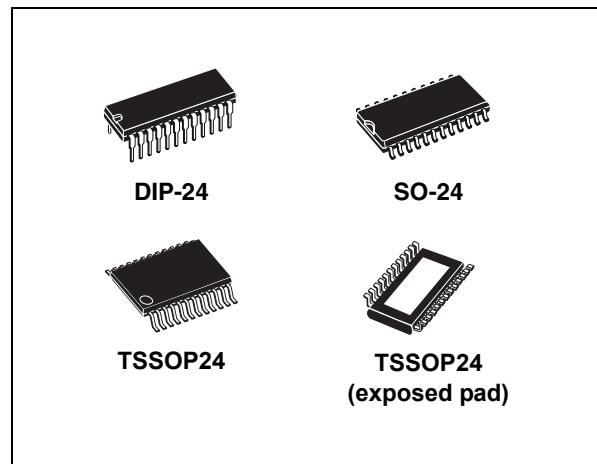


## Low voltage 16-Bit, constant current LED sink driver

### Features

- Low voltage power supply down to 3V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Serial OUT changes state on the falling edges of clock
- 3.3V micro driver-able
- Output current: 3-50 mA
- 25MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad



### Description

The STP16CP596 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CP596 contains a 16-bit serial-IN, parallel-OUT shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources were designed to provide 3-50mA constant current to drive the LEDs.

Compared with the STPIC6C595, the device provides great flexibility and improved performance in LED panel system design.

Users can adjust the STP16CP596 output current with an external resistor, controlling the LEDs' light intensity.

The STP16CP596 guarantees a 16V output driving capability, allowing users to connect more LEDs in series. The high clock frequency (25MHz) also satisfies the high volume data transmission system requirement. The 3.3V voltage supply is useful for applications that interface any microprocessor from 3.3V.

Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a factor of 2:5.

### Order codes

Part number	Package	Packaging
STP16CP596B1R	DIP-24	15 parts per tube
STP16CP596M	SO-24 (Tube)	40 parts per tube
STP16CP596MTR	SO-24 (Tape & Reel)	1000 parts per reel
STP16CP596TTR	TSSOP24 (Tape & Reel)	2500 parts per reel
STP16CP596XTTR	TSSOP24 Exposed-Pad (Tape & Reel)	2500 parts per reel

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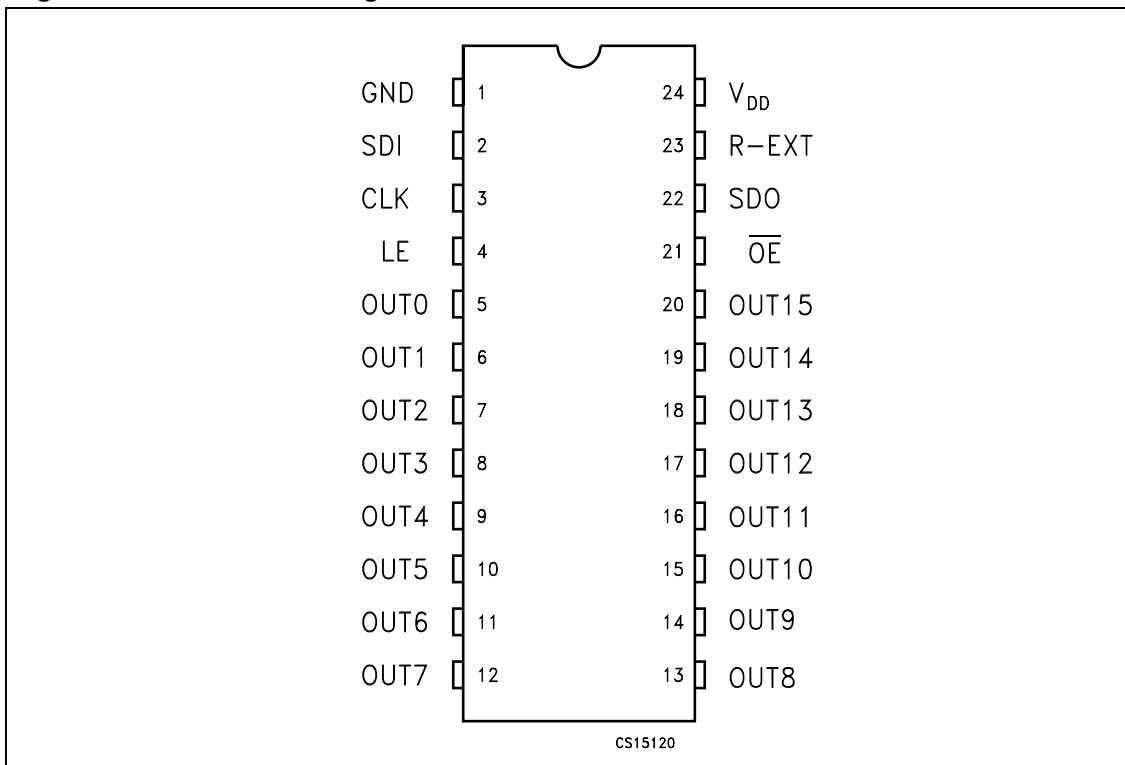
# 1 Summary description

**Table 1. Current accuracy**

Output Voltage	Current accuracy		Between ICs
	Output Current	Between bits	
≥ 0.1V	3mA/V <sub>CC</sub> = 5V	± 3%	± 6%
≥ 0.15V	5mA/V <sub>CC</sub> = 5V	± 2%	± 6%
≥ 0.25V	10mA/V <sub>CC</sub> = 5V	± 2%	± 6%
≥ 0.5V	20mA/V <sub>CC</sub> = 5V	± 1%	± 6%
≥ 1.2V	40mA/V <sub>CC</sub> = 5V	± 1%	± 6%
≥ 1.4V	50mA/V <sub>CC</sub> = 5V	± 1%	± 6%

## 1.1 Pin connection and description

**Figure 1. Connections diagram**



*Note: The Exposed-Pad is electrically not connected*

**Table 2. Pin description**

<b>PIN N°</b>	<b>Symbol</b>	<b>Name and function</b>
1	GND	Ground Terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programming
24	V <sub>DD</sub>	Supply voltage terminal

## 2 Equivalent circuit of inputs and outputs

Figure 2.  $\overline{OE}$  Terminal

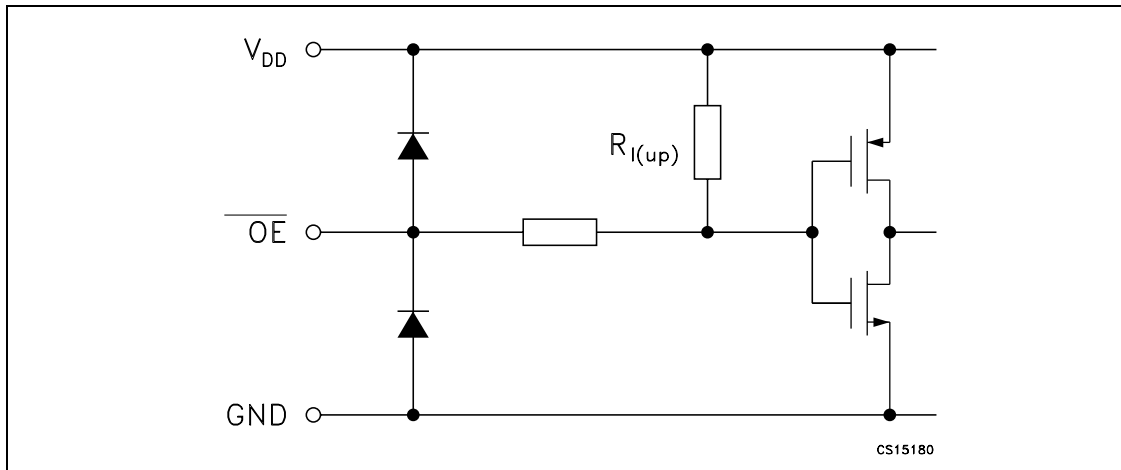


Figure 3. LE Terminal

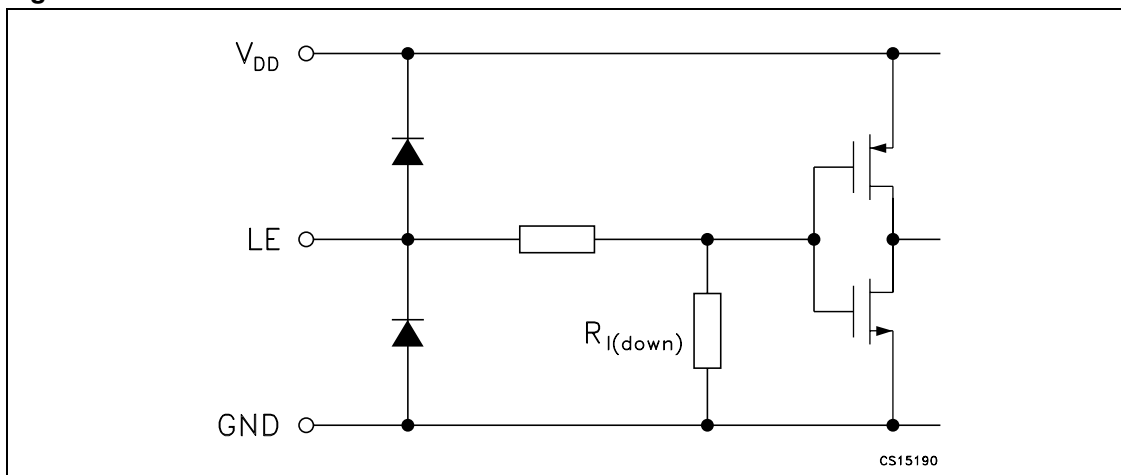


Figure 4. CLK, SDI Terminal

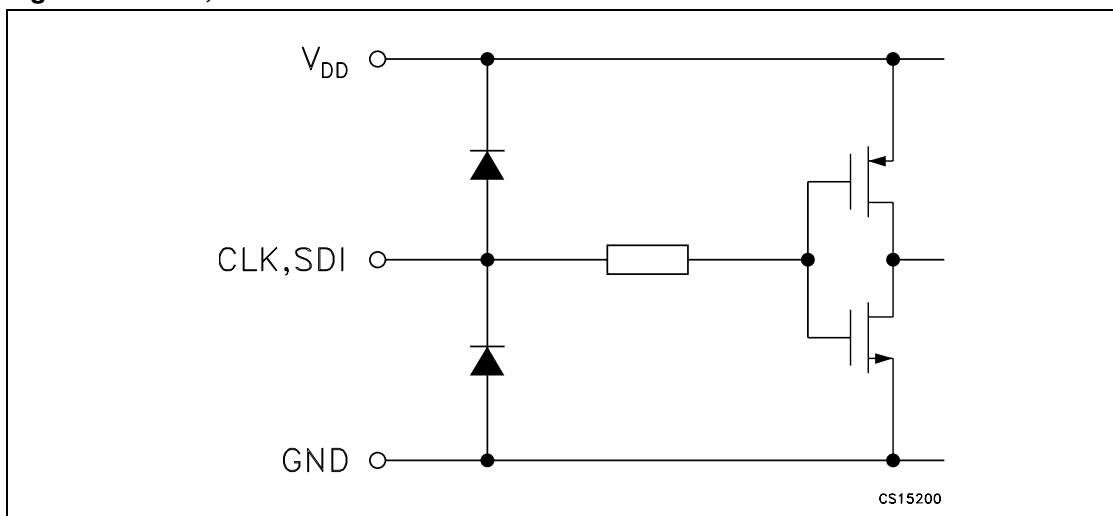


Figure 5. SDO Terminal

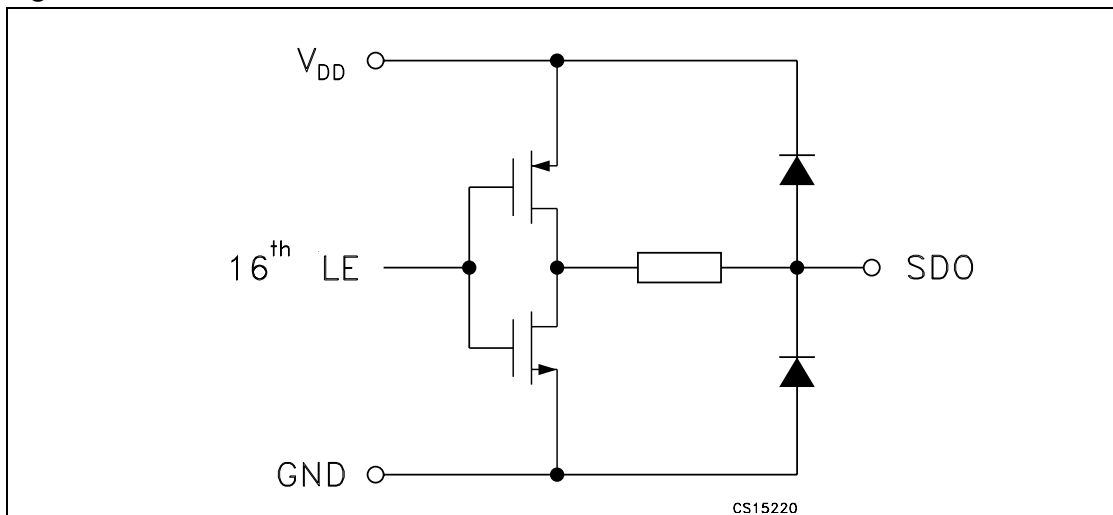
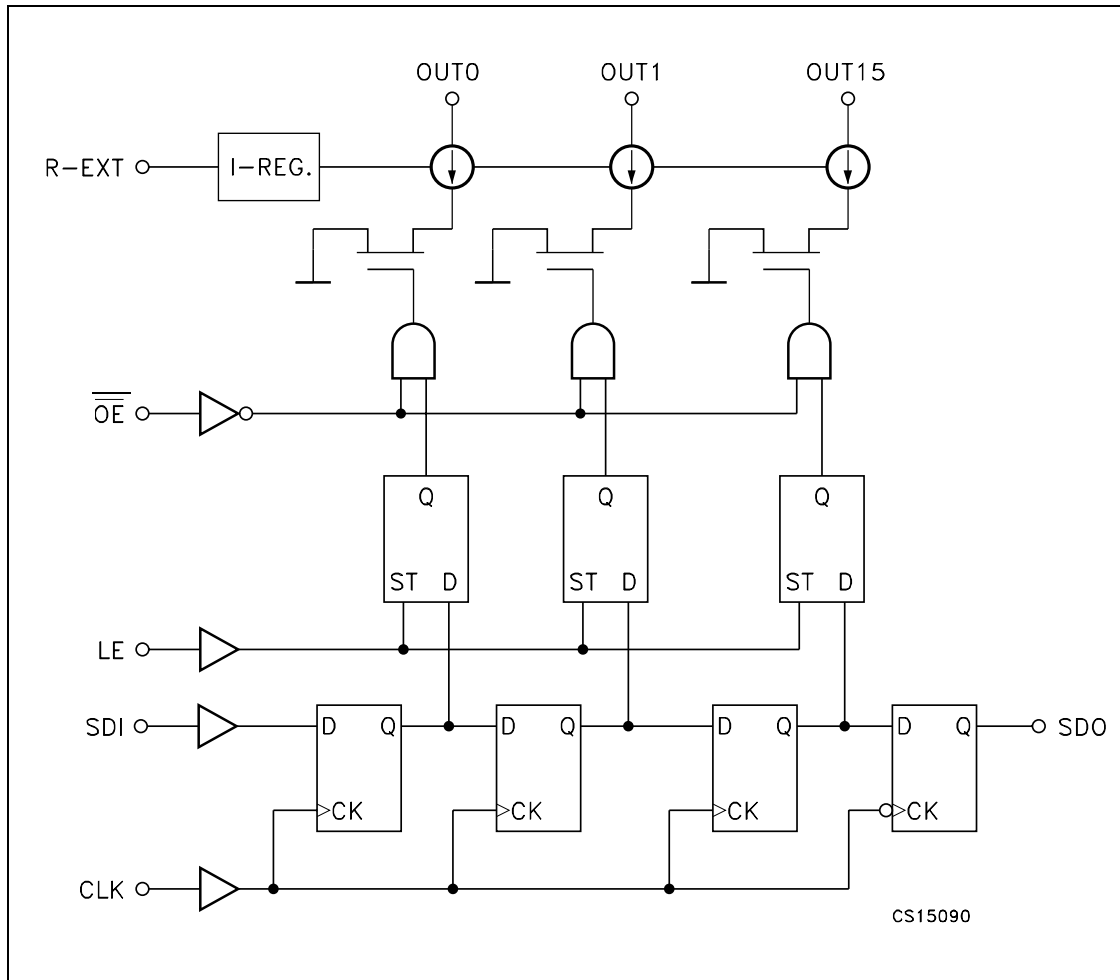


Figure 6. Block diagram - normal mode



## 2.1 Truth table

Table 3. Truth table

Clock	LE	OE	SERIAL-IN	OUT0 ..... OUT7 ..... OUT15	SDO
	H	L	D <sub>n</sub>	D <sub>n</sub> ..... D <sub>n-7</sub> ..... D <sub>n-15</sub>	D <sub>n-15</sub>
	L	L	D <sub>n+1</sub>	No Change	D <sub>n-14</sub>
	H	L	D <sub>n+2</sub>	D <sub>n-2</sub> ..... D <sub>n-5</sub> ..... D <sub>n-13</sub>	D <sub>n-13</sub>
	X	L	D <sub>n+3</sub>	D <sub>n-2</sub> ..... D <sub>n-5</sub> ..... D <sub>n-13</sub>	D <sub>n-13</sub>
	X	L	D <sub>n+3</sub>	ON	D <sub>n-13</sub>

Note: OUT0 to OUT15 = ON when D<sub>n</sub> = H; OUT0 to OUT15 = OFF when D<sub>n</sub> = L.





### 3 Waveforms

Figure 8. Clock, Serial-IN, Serial-OUT

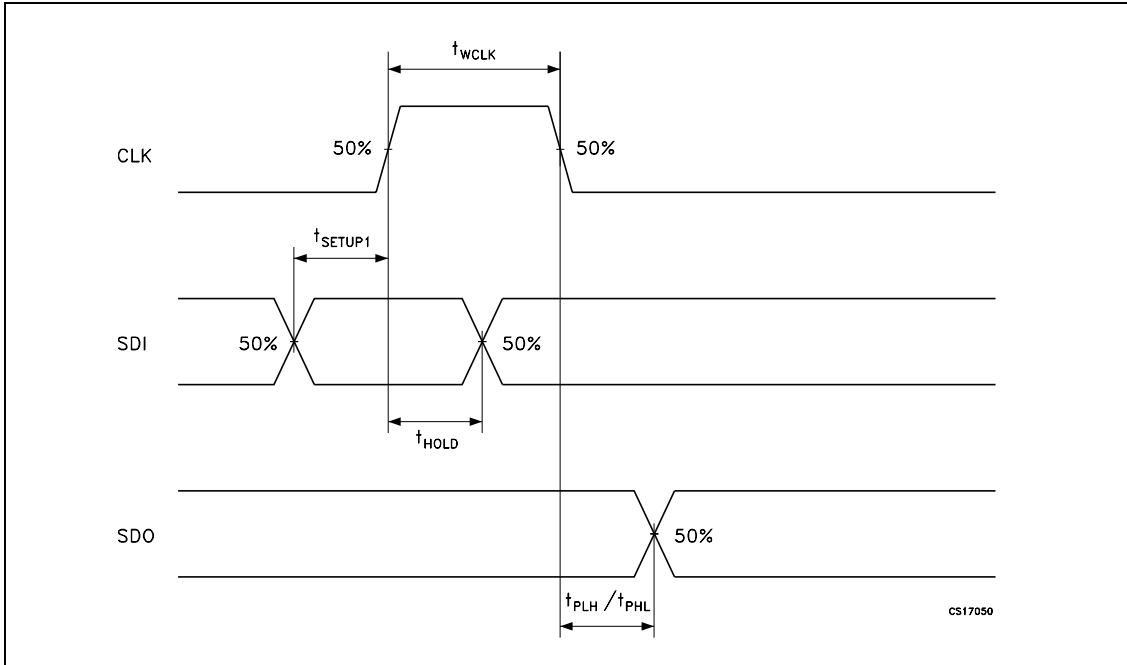


Figure 9. Clock, Serial-In, Latch, Enable, Outputs

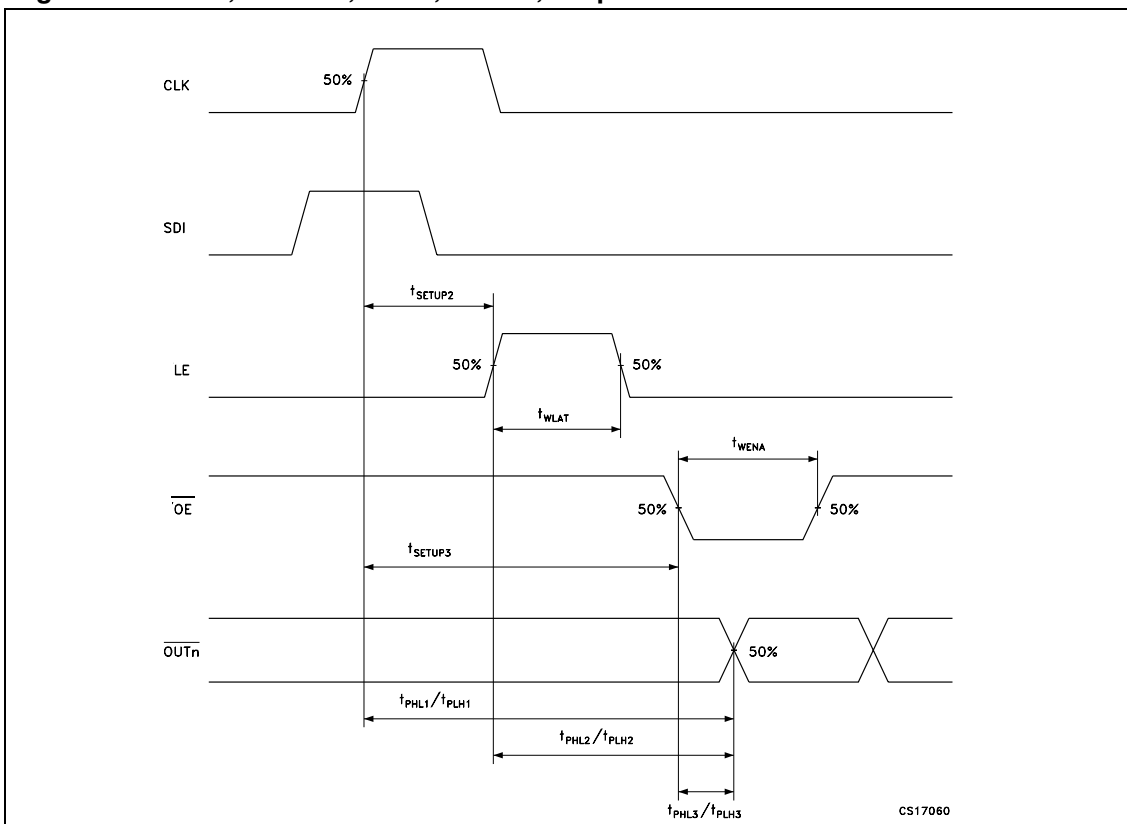
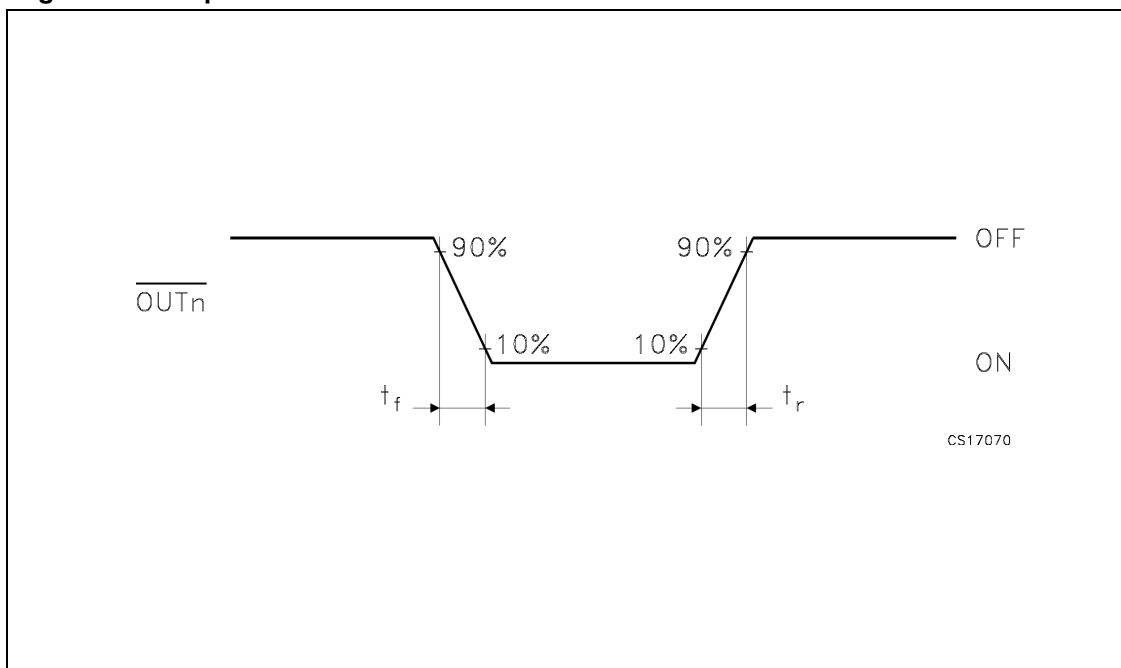


Figure 10. Outputs



## 4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	0 to 7	V
$V_O$	Output Voltage	-0.5 to 16	V
$I_O$	Output Current	50	mA
$V_I$	Input Voltage	-0.4 to $V_{DD}+0.4$	V
$I_{GND}$	GND Terminal Current	800	mA
$f_{CLK}$	Clock Frequency	25	MHz
$T_{OPR}$	Operating Temperature Range	-40 to +125	°C
$T_{STG}$	Storage Temperature Range	-65 to +150	°C

### 4.1 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	DIP-24	SO-24	TSSOP-24	TSSOP-24 <sup>(1)</sup> (exposed pad)	Unit
$R_{thJA}$	Thermal Resistance Junction-ambient	60	75	85	37.5	°C/W

1. The Exposed-Pad should be soldered to the PBC to realize the thermal benefits

## 4.2 Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply Voltage		3.0		5.5	V
$V_O$	Output Voltage				16.0	V
$I_O$	Output Current	OUTn	3		50	mA
$I_{OH}$	Output Current	Serial OUT			+1	mA
$I_{OL}$	Output Current	Serial OUT			-1	mA
$V_{IH}$	Input Voltage		$0.7V_{DD}$		$V_{DD}+0.3$	V
$V_{IL}$	Input Voltage		-0.3		$0.3V_{DD}$	V
$t_{wLAT}$	LE Pulse Width	$V_{DD} = 3.3V$	20			ns
$t_{wCLK}$	CLK Pulse Width		20			ns
$t_{wEN}$	$\overline{OE}$ Pulse Width		400			ns
$t_{SETUP(D)}$	Setup Time for DATA		20			ns
$t_{HOLD(D)}$	Hold Time for DATA		15			ns
$t_{REM(L)}$	Removal Time for LATCH		15			ns
$f_{CLK}$	Clock Frequency	Cascade Operation <sup>(1)</sup>			25	MHz

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

## 5 Electrical characteristics

**Table 7. Electrical characteristics** ( $V_{DD} = 3.3V$  to  $5V$ ,  $T = 25^{\circ}C$ , unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IH}$	Input Voltage High Level		$0.7V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input Voltage Low Level		GND		$0.3V_{DD}$	V
$I_{OH}$	Output Leakage Current	$V_{OH} = 16 V$			10	$\mu A$
$V_{OL}$	Output Voltage (Serial OUT)	$I_{OL} = 1mA$			0.4	V
$V_{OH}$	Output Voltage (Serial OUT)	$I_{OH} = -1mA$	$V_{DD} - 0.4V$			V
$I_{OL1A}$	Output Current	$V_O = \geq 0.2V$ , $R_{EXT} = 6.2K\Omega$ , $V_{DD} = 3.3V$	2.85	3	3.15	mA
$I_{OL2A}$		$V_O = \geq 0.5V$ , $R_{EXT} = 1K\Omega$ , $V_{DD} = 3.3V$	19.6	20	20.4	mA
$\Delta I_{OL1A}$	Output Current Error between bit (All Outputs ON)	$V_O = \geq 0.2V$ , $R_{EXT} = 6.2K\Omega$ , $V_{DD} = 3.3V$		$\pm 4$	$\pm 6$	%
$\Delta I_{OL2A}$		$V_O = \geq 0.5V$ , $R_{EXT} = 1K\Omega$ , $V_{DD} = 3.3V$		$\pm 2$	$\pm 3$	%
$I_{OL1B}$	Output Current	$V_O = \geq 0.2V$ , $R_{EXT} = 6.2K\Omega$ , $V_{DD} = 5V$	2.9	3	3.1	mA
$I_{OL2B}$		$V_O = \geq 0.5V$ , $R_{EXT} = 1K\Omega$ , $V_{DD} = 5V$	19.6	20	20.4	mA
$\Delta I_{OL1B}$	Output Current Error between bit (All Output ON)	$V_O = \geq 0.2V$ , $R_{EXT} = 6.2K\Omega$ , $V_{DD} = 5V$		$\pm 2$	$\pm 3.5$	%
$\Delta I_{OL2B}$		$V_O = \geq 0.5V$ , $R_{EXT} = 1K\Omega$ , $V_{DD} = 5V$		$\pm 1$	$\pm 2$	%
$R_{SIN(up)}$	Pull-up Resistor		150	300	600	$K\Omega$
$R_{SIN(down)}$	Pull-down Resistor		100	200	400	$K\Omega$
$I_{DD(OFF1)}$	Supply Current (OFF)	$R_{EXT} = OPEN$ OUT 0 to 15 = OFF		0.3		mA
$I_{DD(OFF2)}$		$R_{EXT} = 6.2K\Omega$ OUT 0 to 15 = OFF		1		
$I_{DD(OFF3)}$		$R_{EXT} = 1K\Omega$ OUT 0 to 15 = OFF		3		
$I_{DD(ON1)}$	Supply Current (ON)	$R_{EXT} = 6.2K\Omega$ OUT 0 to 15 = ON		1		
$I_{DD(ON2)}$		$R_{EXT} = 1K\Omega$ OUT 0 to 15 = ON		3		

## 6 Switching characteristics

**Table 8. Switching characteristics** ( $V_{DD} = 3.3V$ ,  $T = 25^{\circ}C$ , unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{PLH1}$	Propagation Delay Time, $\overline{CLK}-\overline{OUTn}$ , $LE = H$ , $\overline{OE} = L$	$V_{DD} = 3.3V$ $V_{IL} = GND$ $I_O = 40mA$ $R_{EXT} = 470 \Omega$		250	280	ns	
$t_{PLH2}$	Propagation Delay Time, $LE-\overline{OUTn}$ , $\overline{OE} = L$			220	250	ns	
$t_{PLH3}$	Propagation Delay Time, $\overline{OE}-\overline{OUTn}$ , $LE = H$			200	250	ns	
$t_{PLH}$	Propagation Delay Time, $\overline{CLK}-\overline{SDO}$		$V_{IH} = V_{DD}$ $C_L = 13pF$		25	50	ns
$t_{PHL1}$	Propagation Delay Time, $\overline{CLK}-\overline{OUTn}$ , $LE = H$ , $\overline{OE} = L$		$V_L = 3 V$ $R_L = 65 \Omega$		25	50	ns
$t_{PHL2}$	Propagation Delay Time, $LE-\overline{OUTn}$ , $\overline{OE} = L$				25	50	ns
$t_{PHL3}$	Propagation Delay Time, $\overline{OE}-\overline{OUTn}$ , $LE = H$				50	70	ns
$t_{PHL}$	Propagation Delay Time, $\overline{CLK}-\overline{SDO}$				25	50	ns
$t_{ON}$	Output Rise Time		10 ~ 90% of voltage waveform		260	400	ns
$t_{OFF}$	Output Fall Time	90 ~ 10% of voltage waveform		50	80	ns	

Note: 1 To prevent current overshoot, during the Outputs switching, the overhead output voltage must be less than 1V.

2 The Maximum suggested swithching frequency is up tp 10KHz.

# 7 Test circuit

Figure 11. DC Characteristics

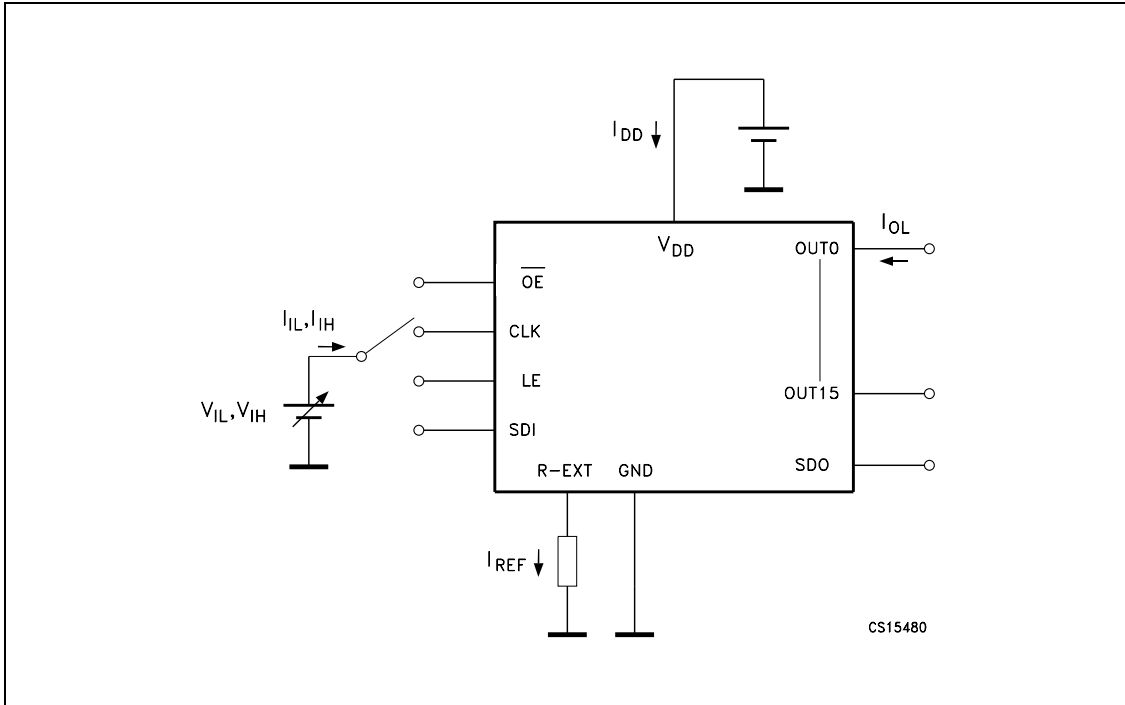
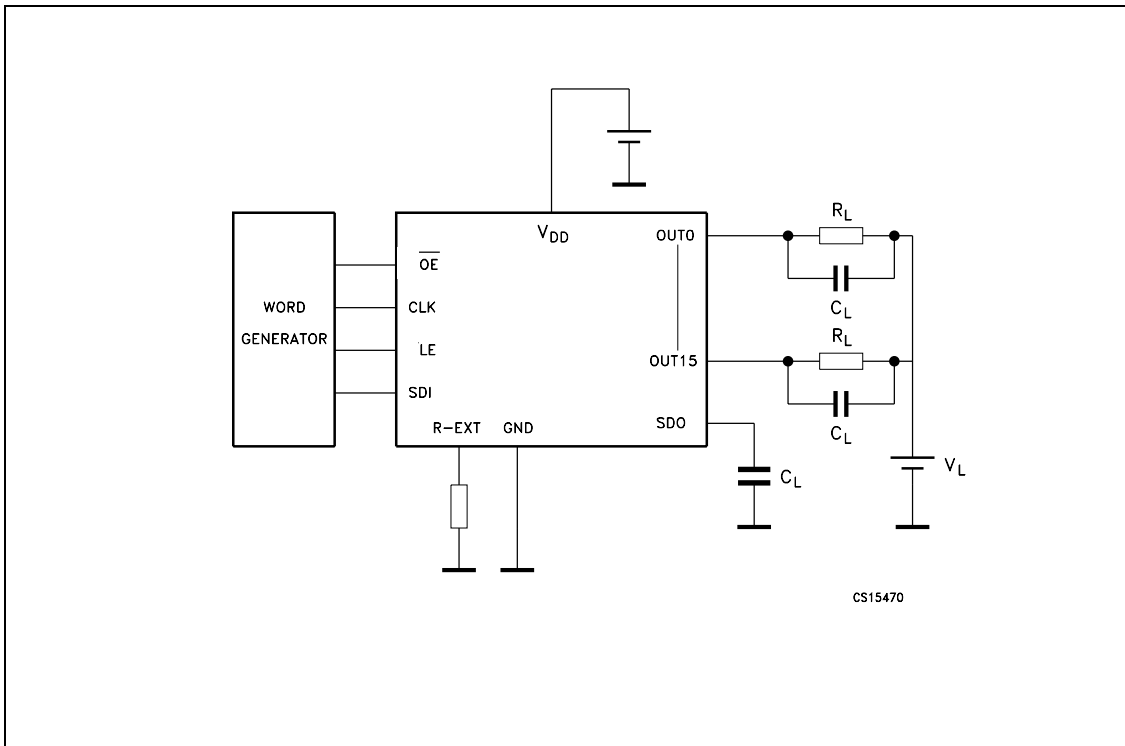
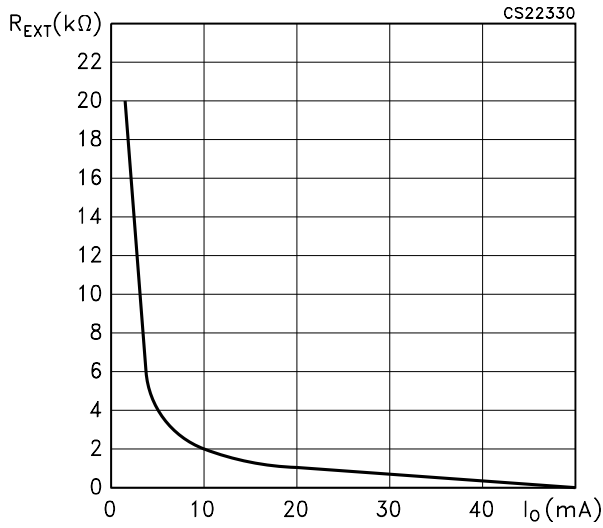


Figure 12. AC Characteristics

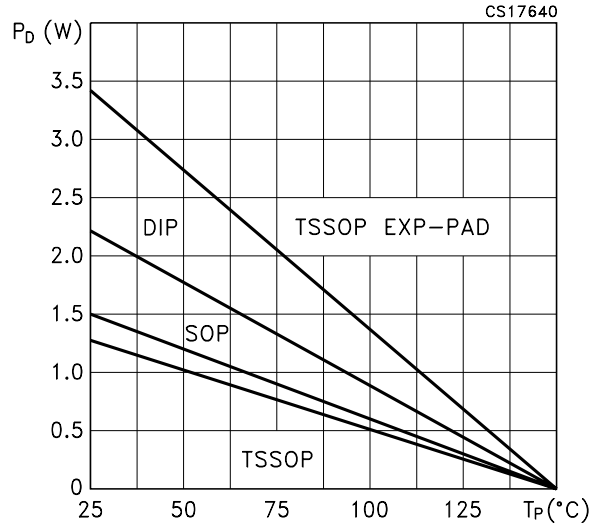


# 8 Typical characteristics

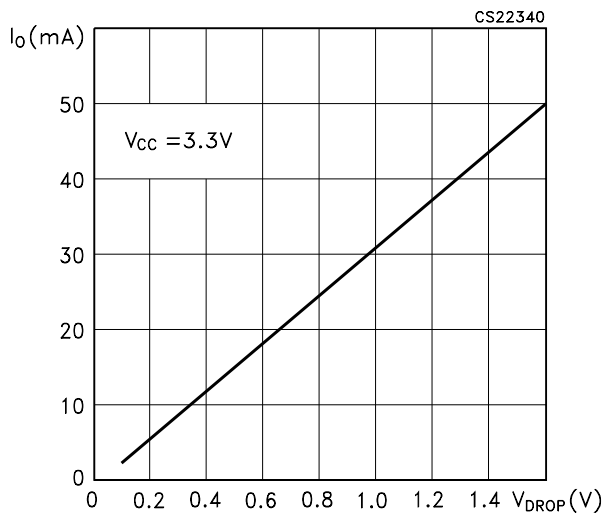
**Figure 13. Output current- $R_{EXT}$  resistor**



**Figure 14. Power dissipation vs. temperature package**



**Figure 15. Output current vs. drop voltage**



**Figure 16. Output current vs  $\pm\Delta I_{OL}$ (%)**

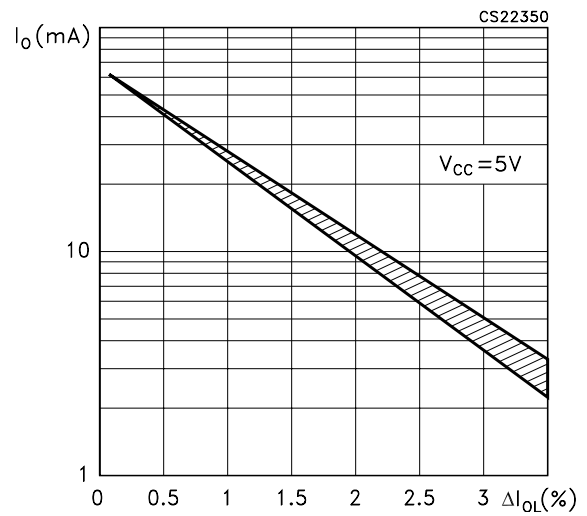
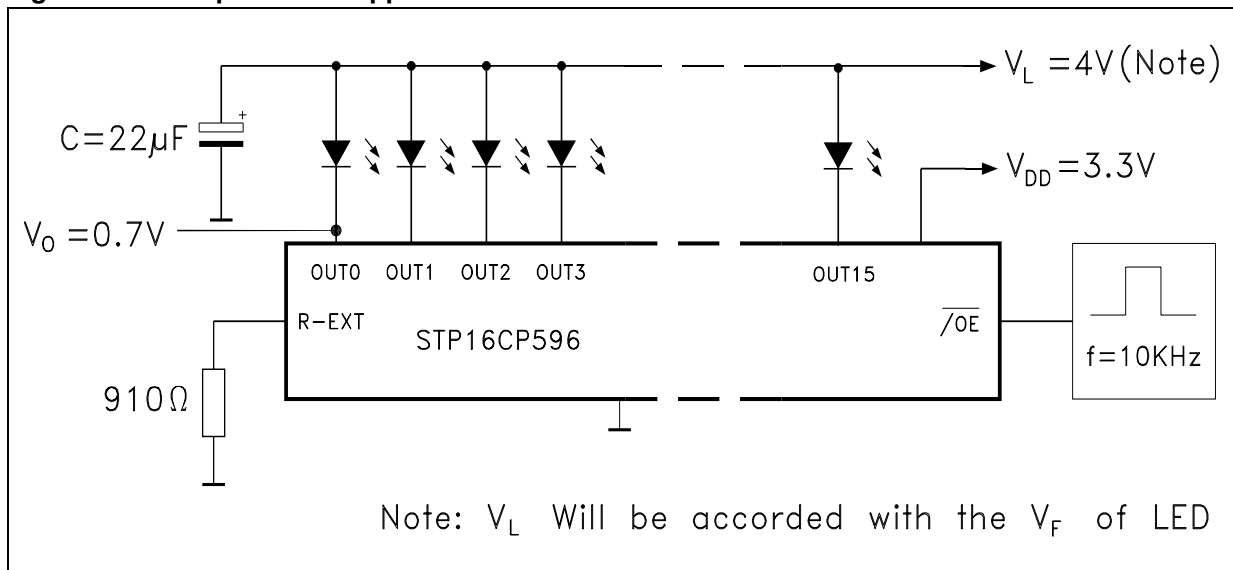




Figure 17. Blue powerLED application circuit



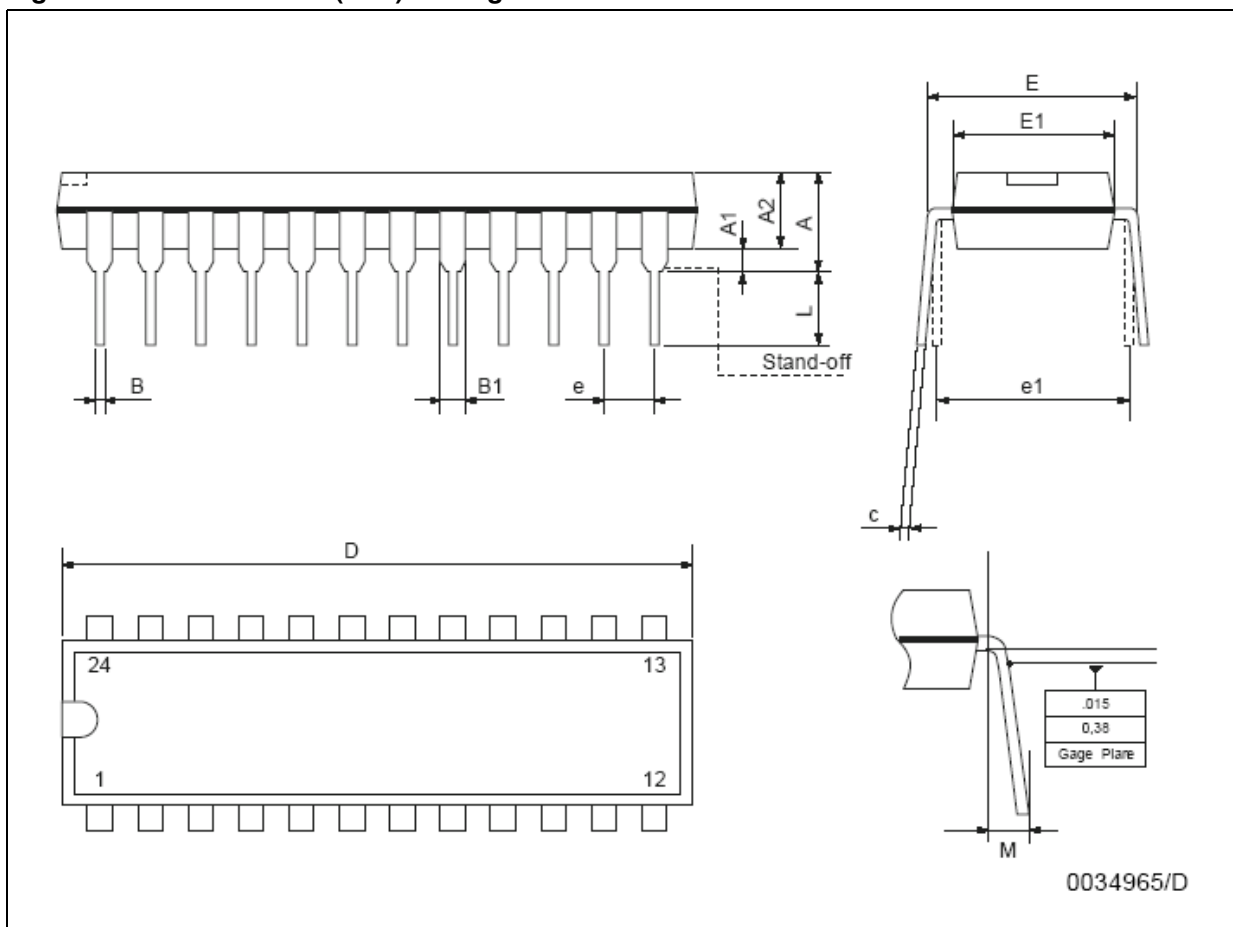
## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

Table 9. Plastic DIP-24 (0.25) Mechanical data

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			4.32			0.170
A1	0.38			0.015		
A2		3.3			0.130	
B	0.41	0.46	0.51	0.016	0.018	0.020
B1	1.40	1.52	1.65	0.055	0.060	0.065
c	0.20	0.25	0.30	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.62		8.26	0.300		0.325
E1	6.35	6.60	6.86	0.250	0.260	0.270
e		2.54			0.100	
E1		7.62			0.300	
L	3.18		3.43	0.125		0.135
M	0°		15°	0°		15°

Figure 18. Plastic DIP-24 (0.25) Package dimensions



**Table 10. TSSOP24 Mechanical data**

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

**Figure 19. TSSOP24 Package dimensions**

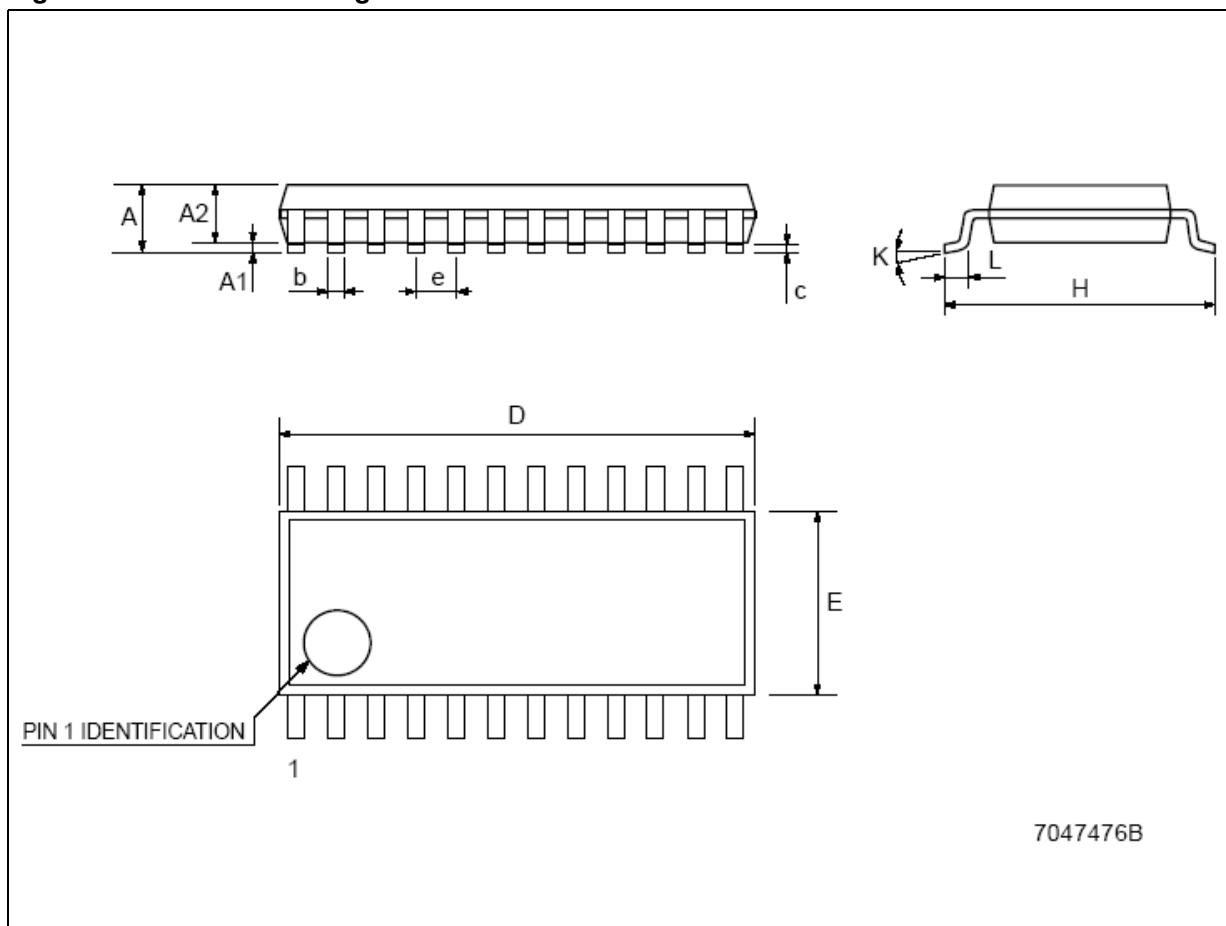


Table 11. Tape & Reel TSSOP24

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 20. Reel dimensions

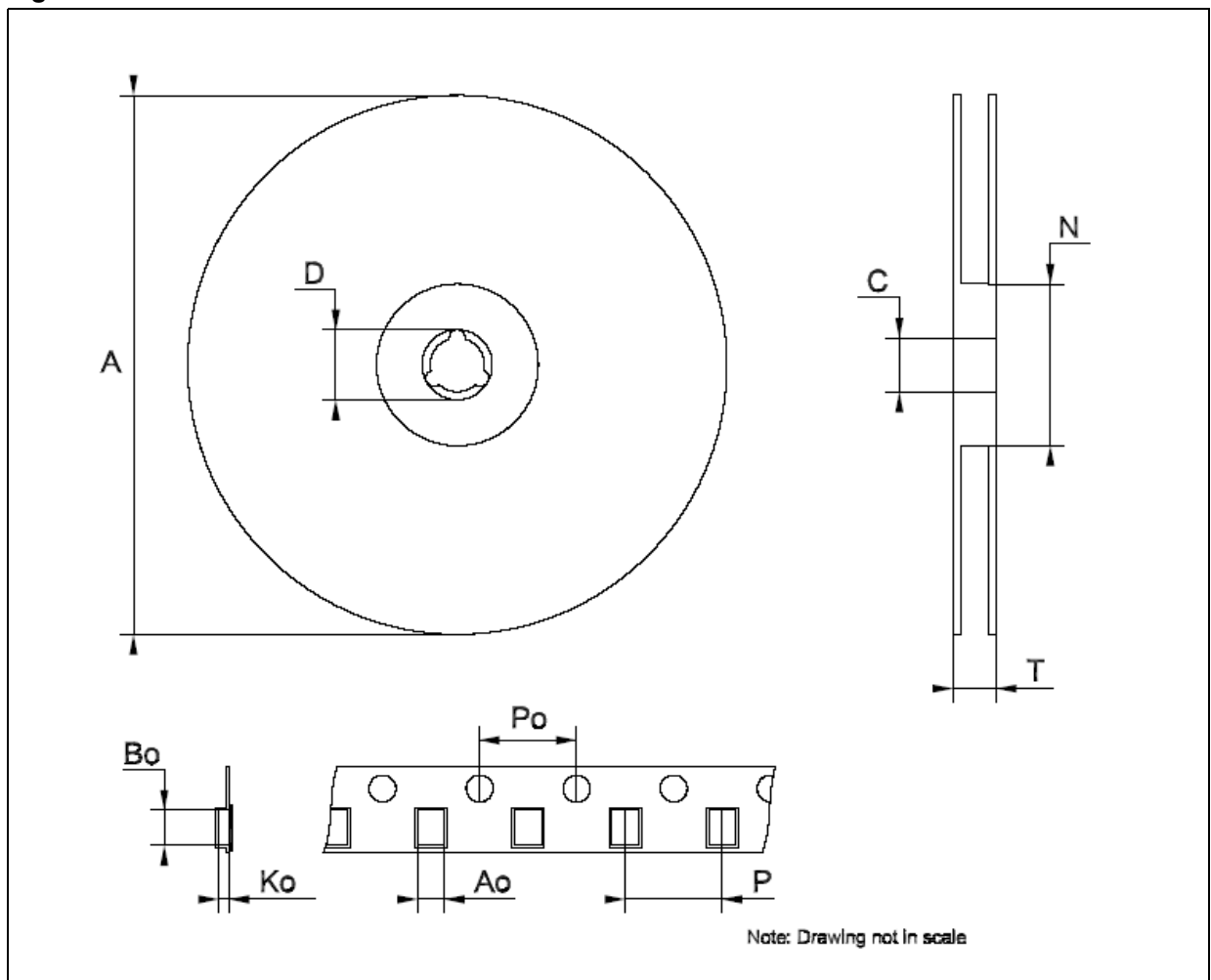
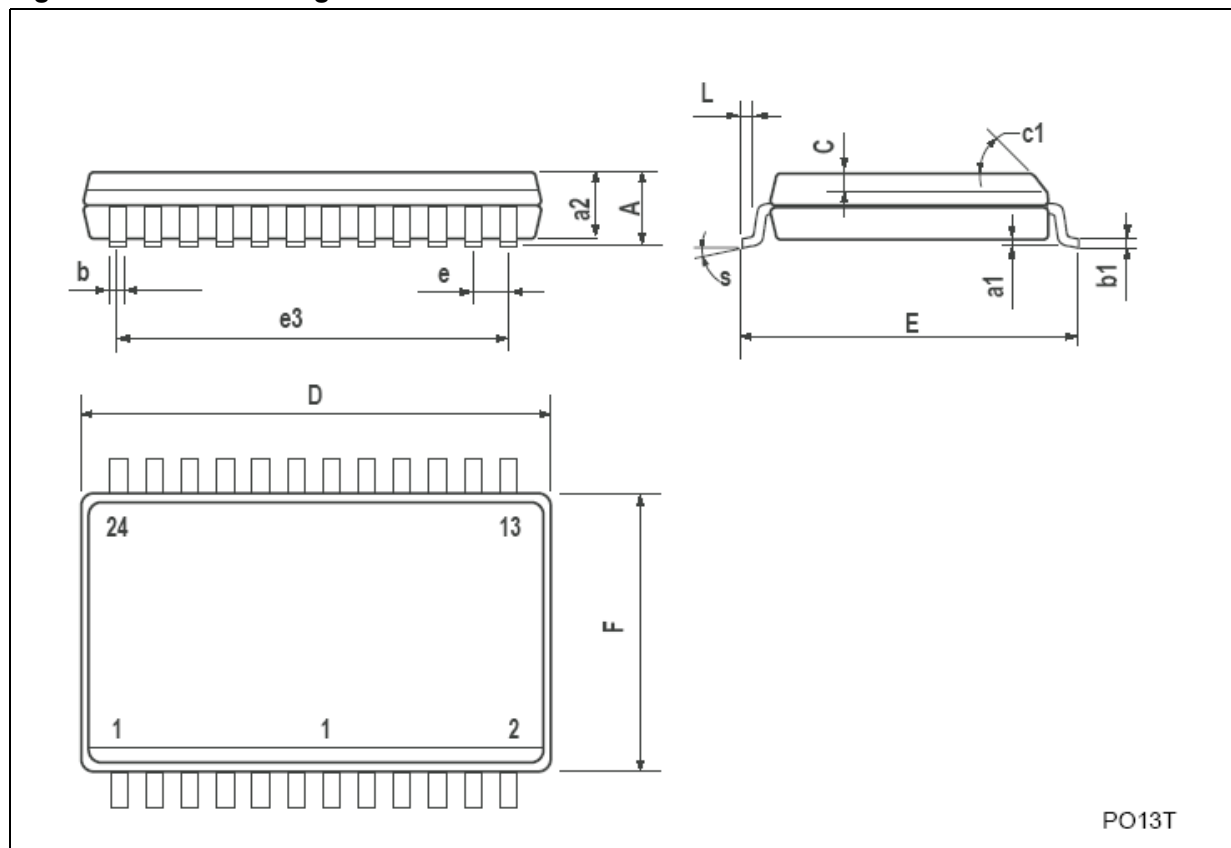


Table 12. SO-24 Mechanical data

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 21. SO-24 Package dimensions



PO13T

Table 13. Tape &amp; Reel SO-24

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	15.7		15.9	0.618		0.626
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 22. Reel dimensions

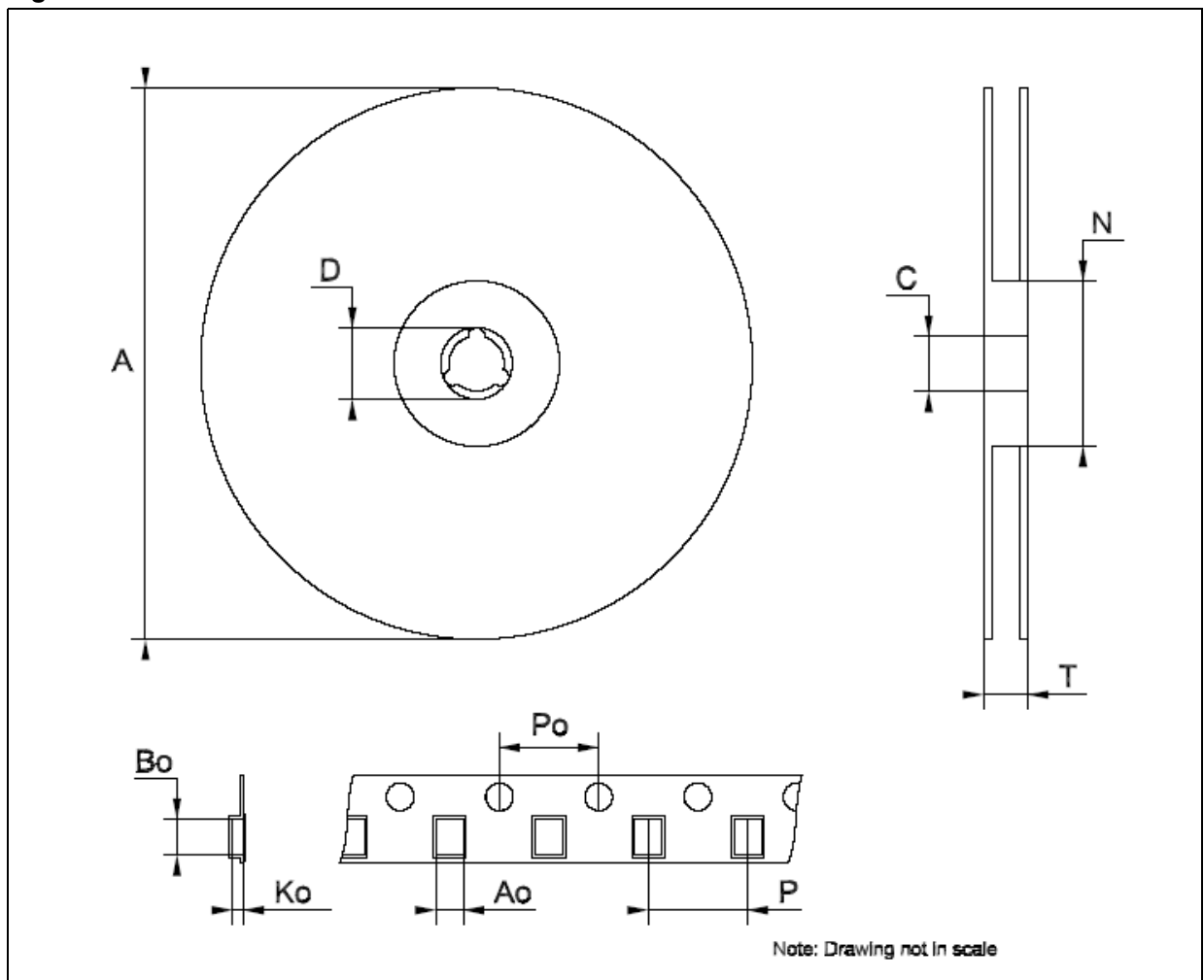
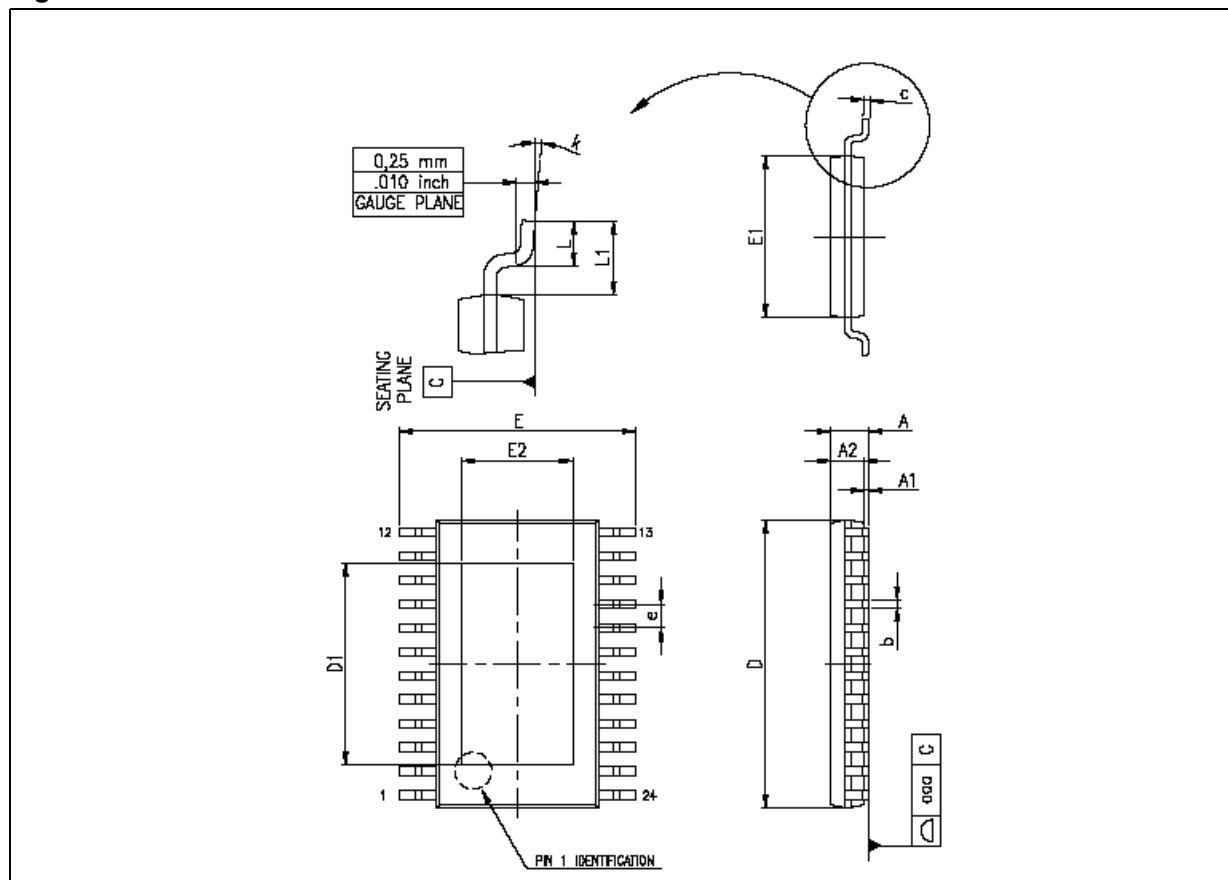


Table 14. TSSOP24 Exposed-pad

Ref	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1		2.7		0.106		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2		1.5		0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 23. TSSOP24 dimensions





## 10 Revision history

**Table 15. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Change</b>
08-Apr-2005	1	First Release.
02-May-2005	2	Typing Error on the description features.
25-Jul-2005	3	Add note on Fig. 1 and Table 5.
16-May-2006	4	New template, few updates

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